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10/019,059	04/19/2002	Damian Dalton	006838-079	8679

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,059	DALTON, DAMIAN	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-3 and 5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-3 and 5-18 have been presented for examination based on amendment filed on 2nd May 2006.
2. Claim(s) 1-3 and 5-18 are amended.
3. Claim(s) 4 is cancelled.
4. The arguments submitted by the applicant have been fully considered. Claims 1-3 and 5-18 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

5. Examiner withdraws objection(s) to specification in view of applicant's amendment to include appropriate headings in the specification.
6. Examiner withdraws the claim objection(s) in view of the applicant's amendment to claim 2 and cancellation of claim 4.
7. Examiner respectfully maintains the objection(s) to drawings until a clean copy of the drawings is filed.
8. Examiner withdraws the claim rejection(s) under 35 USC § 112 to claim 1 in view of the amendment. Rejection is maintained for claim 2 as the language is still vague not providing specific direction when the "count stops".
9. Examiner respectfully withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 1-15 in v0iew of the amendments to claim 1.
10. Examiner withdraws the claim rejection(s) under 35 USC § 102 to claim(s) 1 and 3-18 in view of the amendment. Updated rejection is provided below.

11. Examiner respectfully maintains the claim rejection(s) under 35 USC § 103 to claim(s) 2 in view of the amendment and/or applicant's arguments.

Response to Applicant's Remarks for 35 U.S.C. § 102

12. **Claims 1 and 3-18 are rejected under 35 U.S.C. 102(b) as being anticipated by CompEuro '92 Article "An associative memory approach to parallel logic event-driven simulation" by Damian Dalton (Dalton1992 hereafter).**

Regarding Claims 1 & 16

Applicant has argued that Dalton1992 is not prior art to the current application, however the arguments provided seem to read into the teachings of Dalton1992. Applicant's figure Fig.1 (not marked as prior art) is identical in division of content addressable memory structure as Dalton1992 (Dalton1992: Fig.6). Applicant's arguments are considered and found to be unpersuasive. Please see updated rejection under 35 USC 102 for the amended claims 1 & 16.

Claims 4-15 and 17-18 remain rejected based on their dependency on claims 1 & 16 respectively.

Response to Applicant's Remarks for 35 U.S.C. § 103

13. No new arguments were presented for 35 USC 103 rejection.

Specification

14. Specification is further objected to as it contains program code listing over 300 lines, which should submitted on a compact disc in compliance with 37 CFR 1.96(c).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1 and 3-18 are rejected under 35 U.S.C. 102(b) as being anticipated by CompEuro '92 Article "An associative memory approach to parallel logic event-driven simulation" by Damian Dalton (Dalton1992 hereafter).

Regarding Claim 1

Dalton1992 teaches a *computer implemented* parallel processing method (Dalton1992: Fig.1) of logic simulating comprising representing signals on a line over a time period as a bit sequence, *evaluating gate outputs of the logic gates* including an evaluation of any inherent delay by a *comparing* bit sequences of the inputs of the l*ogic gates* to a predetermined series of bit patterns and in which logic gates whose outputs have changed over the time period are identified during the evaluation of the gate outputs as real gate changes and only *the logic gates having the* real gate changes are propagated to *respective* fan out gates of the logic gates (Dalton1992: Pg.341 Introduction; Pg.342 Bit sequence representation; Pg.342 (vi), (viii)); characterized in that the control of the method is carried out in an associative memory mechanism (1a, 1b) which stores in word form a history of gate input signals by compiling a hit-list register (Dalton1992: Pg.345, Col.1 ¶2) of logic gate state changes and using a multiple response revolver (C) forming part of the

associative memory mechanism (1a, 1b) which generates an address for each hit and then scans and transfers the results on the hit list to an output register for subsequent use (Dalton1992: The Apples System; Fig.6).

Dalton1992 teaches:

> Dividing am associative register into separate smaller associative sub-registers, allocating one type of logic gate to each associative sub-register, each of which associative sub-register has corresponding sub-registers connected thereto, and carrying out gate evaluations and tests in parallel on each associative sub-registers.

As the associative-array (1a & 1b) (Dalton1992: Fig.6 Pg. 345 Col.2 ¶1) which is separated into smaller associative sub-registers, each associated to a logic gate type (Dalton1992: Fig 6, Array 1a; Algorithm – Col.2 assigning & comparing gate type bit pattern for exemplary AND and OR gate). Each of the associative sub-register has corresponding sub-0register connected thereto (Dalton1992: Fig.6 - as Associative array 1a connected to one or more elements in word line register 1b) and carrying out gate evaluation and test in parallel on each associative sub-register (Dalton1992: Pg. 345-346 Algorithm; Fig.1; sub-register 1a denoting a gate type; 345-346, evaluation procedure – "Begin...test size register.. End" section; Col.2 – "Result-Activator-register").

Regarding Claim 3

Dalton1992 teaches the hit list is segmented into a plurality of separate smaller hit-lists (Dalton1992: Pg.345, Col.1 ¶2), each connected to a separate scan register and in which each scan register is operated in parallel to transfer the results to the output register the hit list is *segmented* into a plurality of separate smaller hit lists, each connected to a separate scan register and in which each scan register is *operated in parallel to transfer the results to the output register* (Dalton1992: Pg.345-346, evaluation procedure – "Begin...test size register.. End" section).

Regarding Claim 5

Dalton1992 teaches a method *for comparing* in which each line signal to a target logic gate is stored as a plurality of bits each representing a delay of one time period, *where* aggregate bits representing the delay between signal output to and reception by the target logic gate and in which the inherent delay of each logic gate is represented in the same manner (Dalton1992: Pg 341-343 – "m unit inertial delay model"; Fig.2-3; Pg.344 Col.1-2 Steps (i)-(vi)).

Regarding Claim 6

Dalton1992 teaches each associative sub-register is used to form a hit list connected to a corresponding separate scan register as "group target hit list" (Dalton1992: Pg.345- Col.2).

Regarding Claim 7

Dalton1992 teaches that where the number of one type of logic gate exceeds a predetermined number more than one sub-register is used (Dalton1992: Fig.6- showing more than one sub-registers).

Regarding Claim 8

Dalton1992 inherently teaches that the scan registers are controlled by exception logic using an d OR gate whereby the scan is terminated for each register on the OR changing state then indicating no further match (Dalton1992: Pg.345, Col.1 ¶3; Fig.6).

Regarding Claim 9

Dalton1992 teaches sequentially clearing the hit list and repeating the clearing process inherently (Dalton1992: Pg.345, Col.1 ¶3). Dalton specifically teaches storing the address of the hits (Dalton1992: Pg. 345 Col.1-2)

Pg. 345 Col.1

> **The search is executed simultaneously through all words in the array and a Hit-bit attached to each word indicates successful matches. These hit-bits form a Hit-list-register consisting of a 1 x n column of bits, where n is the number of words.**

Pg. 345 Col.2

> **these changes are applied. These active gates are indicated by a 1 generated by the search in the appropriate bit position of the Group-test-hit-list column register.**

Regarding Claim 10

Dalton1992 teaches each line signal to a target logic gate is stored as a plurality of bits each representing a delay of one time period, the aggregate bits representing the delay between signal output to and reception by the target logic gate (Dalton1992: Pg.343 – Bit sequence representation Fig.2-3).

Regarding Claim 11

Dalton1992 teaches an initialization phase where specified signals are inputted included logic gates (Dalton1992: Pg.343, Test1); unspecified signals are set to unknown or don't cares (Dalton1992: Pg.343, Test2); test templates are prepared defining the delay model of each logic gate (Dalton1992: Pg.342 – bit sequence representation (ii)); input circuit is parsed to generate two-input logic gates (Dalton1992: Pg.342, Col.1 (i)); two level logic gates are then configured (Dalton1992: Pg.342, Col.1 (ii)).

Regarding Claim 12-13

Dalton1992 teaches multi-valued logic is applied and in which n bits are used to represent a signed value at any instance in time with n being any arbitrarily chosen logic (Dalton1992: Pg.342 Col.2 (v)); 8 values logic can also be represented as taught.

Regarding Claim 14

Dalton1992 teaches sequence of values on a logic gate is stored as a bit pattern forming a unique word in the associative memory mechanism (1a, 1b) (Dalton1992: Pg.345, Col.2 ¶1).

Regarding Claim 15

Dalton1992 teaches associative memory storing a record of all values that a logic gate has acquired for the units of delay of the longest delay in the circuit as associative array (1b) storing a record of all values that the logic gate has aquired in each time step with the farthest one indicating the longest delay (Dalton1992: Pg.342 Col2 – Pg.343 Col.2; Fig.2-4).

Regarding Claim 16

Apparatus/Processor claim 16 discloses similar limitations as claim 1 is rejected for the same reasons as claim 1 (Dalton1992: Fig.6).

Regarding Claim 17

Dalton1992 teaches sub-registers as input sub-register, mask sub-register and scan sub-register (Dalton1992: Fig.5).

Regarding Claim 18

Dalton1992 teaches that scan sub-register are connected to an output register (Dalton1992: Pg.345, Col.1 ¶3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE/ CompEuro '92 Article "An associative memory approach to parallel logic event-driven simulation" by Damian Dalton (Dalton1992 hereafter), in view of IEEE article "Model of auto associative memory that stores and retrieves data regardless of their orthogonality, randomness or size" by Bairaktaris, D. (Bairaktaris hereafter).

Regarding Claim 2

Teachings of Dalton1992 are disclosed in claim 1 rejection above.

Dalton1992 does not explicitly teach delay word exceeding the associative register (1b) and storing the gate state in the state register (1a) but provides the identical implementation of the structure of the associative memory as disclosed in the application. Also Dalton1992 teaches variable lengths and types of delays that can be stored in the CAM (Dalton1992: Pg.345 Col.2, ¶1, Lines 5-7).

Bairaktaris teaches storing information in content associative memory where the size of the stored information is greater than the size of the register and illustrates how state register information calculated, until the information is broken down into content-associative-memory-register's size (Bairaktaris: Pg.143-144, Section 3.5, 4.1).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Bairaktaris to Dalton1992 to divide the delay information if it exceeds the associative register word width. The motivation to combine would have been that Bairaktaris teaches creating auto

associative content addressable memory (CAM) where the size to be stored is greater than the size of the register (Bairaktaris: Introduction). Further, Bairaktaris teaches CAM to be shared CAM (Bairaktaris: Introduction) which Dalton1992 uses to implement the CAM accessed by multiple processors (Dalton1992: Fig.1 Pg.354 Apples system – parallel operations). Similar prior art addressing the overflow in the CAM was also available at the time of instant application[1].

[1] U.S. Patent Nos. 5423015, 6226710.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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